WHAT IS CLAIMED IS:

1. A memory, comprising:

an array of magnetic memory cells, each magnetic memory cell being adapted to store a bit of information;

interconnects in communication with the magnetic memory cells; and

conductors in communication with the magnetic memory cells and the interconnects, the conductors filling spaces between adjacent magnetic memory cells of the array.

2. The memory of claim 1, wherein the conductors comprise top conductors formed by a patterning process that also patterns the magnetic memory cells.

3. The memory of claim 1, further comprising a substrate, wherein the array of magnetic memory cells is supported on the substrate and wherein the interconnects pass at least partially through the substrate.

4. The memory of claim 1, wherein at least one of the conductors is deposited on at least one of the interconnects and at least one other of the conductors is deposited on at least one of the magnetic memory cells.

5. The memory of claim 1, wherein the conductors comprise top conductors, the memory further comprising bottom conductors disposed generally orthogonally to the top conductors, each bottom conductor supporting multiple magnetic memory cells of the array.

6. The memory of claim 5, wherein the top conductors are deposited between the bottom conductors and between adjacent magnetic memory cells of the array.

7. The memory of claim 1, wherein the magnetic memory cells each comprise an active layer having a non-fixed magnetization and a reference layer having a fixed magnetization.

8. The memory of claim 1, wherein the conductors filling spaces between adjacent magnetic memory cells of the array are top conductors disposed between bottom conductors of the array and between the adjacent magnetic memory cells.

9. The memory of claim 1, wherein the conductors comprise top conductors, the memory further comprising:

bottom conductors in communication with the magnetic memory cells; and

a dielectric material disposed between the top conductors and the bottom conductors.

10. The memory of claim 9, wherein the dielectric material insulates the magnetic memory cells.

11. The memory of claim 1, wherein each magnetic memory cell comprises a patterned stack; the memory further comprising a dielectric layer disposed on sides of the patterned stack.

12. The memory of claim 11, wherein the dielectric layer is disposed on sides of the conductors.

13. A method of making an electronic memory comprising a first conductor formed on a substrate, the first conductor contacting a first post extending at least partially through the substrate, the method comprising:

depositing storage cell material on the first conductor;

depositing a protective layer on the substrate and the storage cell material;

removing a portion of the protective layer from the substrate such that the remaining protective layer overlies the substrate only immediately adjacent a

perimeter of the storage cell material, the removing causing a second post extending at least partially through the substrate to be exposed; and

patterning second conductors on the storage cell material and on the second post.

14. The method of claim 13, wherein the patterning also patterns the storage cell material to form a plurality of storage cells on the first conductor.

15. The method of claim 14, wherein the patterning patterns the storage cell material in one dimension; the method further comprising patterning the first conductor, wherein patterning the first conductor patterns the storage cell material in another dimension.

16. The method of claim 13, wherein the patterning comprises forming storage cells from the storage cell material, wherein adjacent storage cells define intervening spaces bordered by the first conductor.

17. The method of claim 16, further comprising depositing second-conductor material forming the second conductors to generally fill the spaces between adjacent storage cells.

18. The method of claim 13, further comprising depositing second-conductor material forming the second conductors on the storage cell material and over the second post generally simultaneously.

19. The method of claim 13, wherein the patterning patterns an active layer of the storage cell material.

20. The method of claim 19, wherein the patterning patterns a reference layer and a dielectric region of the storage cell material.

21. A memory, comprising:

means for storing information having logic states, the means for storing comprising a plurality of storage units defining intervening gaps between adjacent storage units; and

means for sensing the logic states of the means for storing;

wherein the means for sensing fills the intervening gaps of the means for storing.

22. The memory of claim 21, wherein the means for sensing comprises a plurality of top conductors and a plurality of bottom conductors extending generally orthogonally to the plurality of top conductors.

23. A memory structure, comprising:

magnetic cells deposited on first conductive layers, the magnetic cells in communication with first vias of the memory structure;

insulating layers deposited on sides of the magnetic cells and patterned edges of the first conductive layers; and

second conductive layers deposited over the insulating layers and the magnetic cells, the second conductive layers overlying second vias of the memory structure.

24. The memory structure of claim 23, wherein the second conductive layers fill gaps between adjacent magnetic cells.

25. The memory structure of claim 23, wherein multiple magnetic cells are deposited on a common first conductive layer.

26. The memory structure of claim 23, further comprising multiple conductors formed from the second conductive layers.

27. The memory structure of claim 26, wherein the multiple conductors directly contact the magnetic cells and directly overlie the second vias.